Logical operations with Localized Structures

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Localized structures (LS), also known as dissipative solitons, have been suggested as a potentially useful strategy for information storage. This application is specially attractive in nonlinear photonics after LS have been observed in semiconductor lasers, but the general concept of using LS to carry information is not restricted to optics. Within this approach a LS describes one bit of information. This idea can be taken a step further and discuss the potential of LS for carrying out computations beyond mere information storage. In this work we propose to use excitability mediated by LS to implement three basic logic gates, namely the AND, OR, and NOT gates, providing complete logic functionality[1], as by combination of them one can realize any other logical operation, including the NOR and NAND universal gates. In our scheme bits are represented by a dynamical state (an excitable excursion) rather than by a stationary solution. This provides a natural reset mechanism for the gates. The way computations are performed relays on the emergent properties of the LS, independently of the microscopic details of the underlying physical system.

We consider a nonlinear optical cavity as sketched in Fig. 1. Three narrow addressing beams b_1, b_2, and b_3 facilitate excitability by allowing to tune the threshold for the size of a perturbation necessary to trigger an excitable excursion. The positions in the transverse plane of these narrow beams define also the input and output ports of the logic gate. Alternatively the transverse plane of the device could be engineered to fix the positions of the ports. Here the bright spots created inside the cavity by b_1 and b_2 will act as input ports, while the spot at the position of b_3 will be the output port. The incoming bits (δ_1, δ_2) will be superimposed to b_1, b_2.

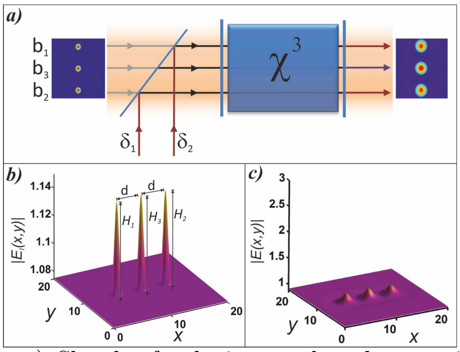

FIG. 1. a) Sketch of a logic gate based on excitable LS in a nonlinear optical cavity. b) Input of the cavity $E_I(x, y)$, including the holding beam (background) and the three localized beams with intensities H_1, H_2, and H_3. d is the distance between ports. c) Intracavity field of the resting state of the system. Adimensional units are used in all figures.

In our proposal a bit '1' corresponds, internally, to the presence of an excitable excursion. Then, a superthreshold perturbation at an input port (i.e. causing an excitable excursion) will be considered as a bit '1', while sub-threshold (or absence of) perturbations will be considered as '0'. At the output port, the occurrence of an excitable excursion should be taken as a '1', and '0' otherwise.

For an OR gate, d and H_3 are such that an excitable excursion of a single input is already enough to excite the output, as shown in Fig. 2. The bit '1' is introduced by setting $\delta_1 = 0.03$ during 1 time unit. After receiving the bit, the left input port exhibits an excitable excursion which, by the above mechanism, triggers an excitable excursion of the output port. Because of symmetry, the output would look exactly the same for the case (0,1). A double activated (1,1) input would give a very similar response, completing the truth table of the OR gate.

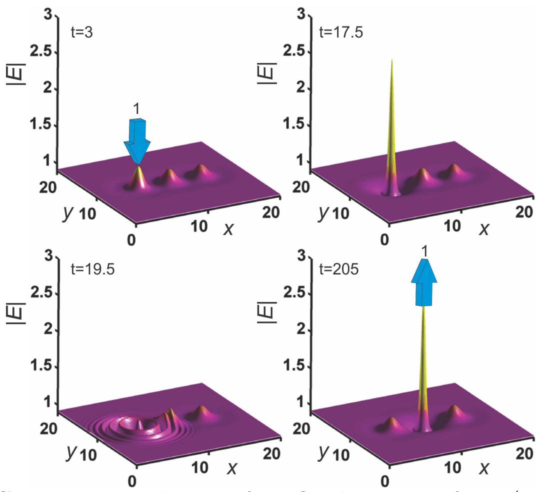

FIG. 2. Time evolution of an OR logic gate for a (1,0) input.

Similarly, AND logic can be implemented by increasing d or decreasing H_3, such that the pulse of a single input is not enough to elicit a response of the output, but the combined action of two simultaneous excitations is. A NOT gate is also proposed, providing together with the OR and AND gates full logic functionality.

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[1] A. Jacobo, D. Gomila, M.A. Matías, and P. Colet, New Journal of Physics **14**, 013040 (2012).